UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/595,034	01/05/2006	Mattias Nilsson	P17494-US1	1623

27045 7590 07/31/2006

ERICSSON INC.
6300 LEGACY DRIVE
M/S EVR C11
PLANO, TX 75024

EXAMINER	
GIRARDI, VANESSA MARY	
ART UNIT	**PAPER NUMBER**
2833	

DATE MAILED: 07/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/595,034	NILSSON ET AL.	
	Examiner	Art Unit	
	Vanessa Girardi	2833	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05 Jan 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C.§103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 10-13 are rejected under 35 U.S.C. §103(a) as being unpatentable over Smolley (US 4,581,679) and Higgins III (US 5,117,069) in further view of Boegh-Petersen (US 4,707,657).

With respect to claim 10; Smolley shows an arrangement of stacked circuit boards (Fig. 3), comprising: arranging at least two circuit boards **10**, **12** having a pair of opposing circuit board terminals **14** and a first retainer board **16** having at least one hole **18** into which a wire button contact **20** is inserted, the wire button contact **20** providing electrical connection between the pair of opposing circuit board terminals **14** of the two circuit boards **10**, **12**.

However Smolley does not show the hole being plated and at least one conductor connected to the hole.

Higgins III shows an arrangement of stacked circuit boards (Fig. 1) having at least one plated hole **111** and at least one conductor **128** connected to the hole.

However neither Smolley nor Higgins III show a method of testing an arrangement of stacked circuit boards.

Boegh-Petersen shows an arrangement of stacked circuit boards (Figs. 1-6) employing a method for producing and testing such an arrangement (Col. 2, lines 25-54).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made that plating the through hole of Smolley as taught by Higgins III would

provide for redundant assurance of connectivity between the printed circuit boards while also permitting external access to the through hole by way of a conductor. All of which would serve to easily test the circuit boards for electrical integrity that is not otherwise validated through visual inspection as taught by Boegh-Petersen, thus being able to ascertain acceptability of the printed circuit board components prior to their final assembly; thus saving time, money and producing a more reliable product in having electrically inspected the printed circuit boards.

With respect to claim 11; Smolley shows fixedly assembling the printed circuit board arrangement (Col. 6, lines 5-21).

With respect to claim 12; Smolley shows it is well-known through the prior art as an example that the retainer board **16** is a multilayer board (Col 2, lines 15-18) wherein dielectric layers constitute the outer layers (Col. 1, lines 50-55) of a mid section of the multilayer retainer board.

With respect to claim 13; Smolley shows inserting a second retainer board **32** which is substantially identical to the first retainer board (Fig. 3).

2. Claims 14 and 15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Smolley (US 4,581,679) In view of Higgins III (US 5,117,069).

With respect to claim 14; Smolley shows at least two circuit boards **10**, **12** having a pair of opposing substrate terminals **14**, a first retainer board **16** having at least one hole **18** into which a wire button contact **20** is inserted, the wire button contact **20** providing electrical connection between the pair of opposing circuit board terminals **14** of the two circuit boards **10**, **12**.

However Smolley does not show the hole being plated and at least one conductor connected to the hole.

Higgins III shows an arrangement of stacked circuit boards (Fig. 1) having at least one plated hole **111** and at least one conductor **128** connected to the hole.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made that plating the through hole of Smolley as taught by Higgins III would provide for redundant assurance of connectivity between the printed circuit boards while also permitting external access to the through hole by way of a conductor enabling the ability to ascertain acceptability of the printed circuit board components prior to their final assembly; thus saving time, money and producing a more reliable product in having electrically inspected the printed circuit boards.

With respect to claim 15; Smolley shows the retainer board **16** is a multilayer board (Col. 2, lines 15-18) wherein dielectric layers constitute the outer layers (Col. 1, lines 50-55) of a mid section of the multilayer retainer board.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vanessa Girardi: Telephone number (571) 272-5924.

Monday – Thursday 7 a.m. to 5:30 p.m. (EST)

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paula Bradley can be reached on (571) 272-2800 ext 33.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VG
Art Unit 2833
July 17, 2006

THO D. TA
PRIMARY EXAMINER